Remarks

A. Pending Claims

Claims 1-7, 11, 13-15, and 20-28 are currently pending. Claims 21-28 are withdrawn. Claims 1-7, 11, 13-15, and 20 are rejected. Claim 12 has been cancelled. Claims 1, 20, and 21 have been amended.

B. Election/Restriction

The Office Action states: "New claims 21-28 are non-elected because they lack the same or corresponding special technical features such as claim 1 does not require providing the buried layer after the source and drain are formed as in claim 21." Applicant respectfully disagrees.

Amended claim 21 states:

> A method for manufacturing a semiconductor device, comprising:
>
> forming, in a silicon body, source and drain regions defining between them a channel region;
>
> providing a thin gate dielectric layer on the channel region and a gate on the thin gate dielectric layer; and
>
> providing a buried layer of a dielectric and a thin silicon layer extending between the source and drain regions and lying between the buried dielectric layer and the gate dielectric layer, said buried layer being underneath said source and drain regions, wherein the thin silicon layer has an area greater than that of the gate dielectric layer so that its upper surface comprises two opposed zones which extend beyond the gate dielectric layer and in that the source and drain regions each overlap respectively, at least in part, one of said opposed zones, and wherein the thin silicon layer has a thickness between about 1 nm and about 50 nm.

Applicant submits that the order of the features of the claims does not correspond to a chronological order for performing the method. Applicant has amended claim 21 for

clarification. Applicant submits no new matter has been added to the specification.

As such, Applicant submits that claim 21 and the claims dependent thereon (claims 22-28) have corresponding special technical features to claim 1 and the claims dependent thereon (claims 2-7, 11, and 13-15).

Applicant respectfully requests that claims 21-28 be examined.

C. The Claims Are Not Anticipated By Assaderaghi et al. Pursuant To 35 U.S.C. § 102(e)

Claims 1, 3, 6, and 7 were rejected as being anticipated by U.S. Patent No. 6,686,629 to Assaderaghi et al. (hereinafter "Assaderaghi"). Applicant respectfully disagrees with these rejections.

The standard for "anticipation" is one of fairly strict identity. A claim can only be anticipated if each and every element set forth in the claims is found to be either expressly or inherently described in the cited art. *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 728, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), MPEP § 2131.

Amended claim 1 describes a semiconductor device that includes a combination of features including, but not limited to, the feature of: "wherein the thin silicon layer has a thickness between about 1 nm and about 50 nm". Support for the amendment is found in original claim 12.

Assaderaghi does not appear to teach or suggest a thin silicon layer having a thickness between about 1 nm and 50 nm. Assaderaghi appears to teach a silicon layer of n-type or p-type. Assaderaghi states, "The silicon layer 3 can be doped either in n-type or p-type" (Column 4, lines 27 and 28).

The Office Action states: "However it would have been obvious of one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal values or ranges for the thickness of the buried dielectric layer, the thickness of silicon channel layer...."

Applicant's specification states: "Thus, even with extremely small thicknesses of the thin silicon layer 13, a reliable and sufficient contact is made between the source and drain regions 23, 24 and the thin silicon layer 13 constituting the channel, which could not be the case with a simple lateral contact." (Specification, Page 6, lines 17-20).

Although, Assaderaghi describes a silicon layer, Applicant submits that Assaderaghi does not appear to provide guidance in regards to the thickness of the silicon layer. Applicant submits that it is not obvious to one of ordinary skill in the art that a silicon layer having a thickness between about 1 nm and 50 nm will ensure a reliable and sufficient contact between the source and drain regions.

Portions of the aforementioned rejection appear to be set forth in facts within the personal knowledge of the Examiner and therefore Applicant believes MPEP 2144.03 will apply. Pursuant to MPEP 2144.03, Applicant respectfully requests the Examiner to provide support for his assertion either by an affidavit or by references brought to the Applicant's attention. Otherwise, Applicants request this rejection be removed. *See, e.g.,* MPEP 2143.01.

Applicant further submits that the independent claims include, but are not limited to the feature of "the thin silicon layer has an area greater than that of the gate dielectric layer so that its upper surface comprises two opposed zones which extend beyond the gate dielectric layer and in that the source and drain regions each overlap respectively, at least in part, one of said opposed zones." Applicant respectfully submits that this feature is neither taught nor suggested by Assaderaghi. Specifically, Applicant directs the Examiner's attention to FIG. 1 of Assaderaghi. FIG. 1 appears to show that silicon layer 3 has a top surface that does not extend beyond the gate dielectric layer. In fact, the top

surface of the silicon layer (3) appears to have the same width as the gate dielectric layer (4).

Applicant submits, therefore, that the combination of features of the independent claims does not appear to be taught or suggested by Assaderaghi. As such, Applicant submits that claim 1 and the claims dependent thereon are patentable over Assaderaghi.

The Examiner is also respectfully requested to separately consider each of the dependent claims for patentability. Many of the dependent claims in addition to those mentioned above are independently patentable.

Claim 3 states in part, "wherein the buried dielectric layer extends over the entire surface of the silicon body below the source and drain regions." Applicant submits that the features of claim 3 in combination with the features of independent claim 1 do not appear to be taught or suggested by Assaderaghi.

Claim 6 states in part, "wherein the buried dielectric layer is a solid material." Applicant submits that the features of claim 6 in combination with the features of independent claim 1 do not appear to be taught or suggested by Assaderaghi.

Claim 7 states in part, "wherein the device is a transistor." Applicant submits that the features of claim 7 in combination with the features of independent claim 1 do not appear to be taught or suggested by Assaderaghi.

Applicant respectfully requests the removal of the rejections for claim 1 and the claims dependent thereon (claims 2-7, 11, and 13-15).

D. <u>The Claims Are Not Obvious Over Assaderaghi In View of Schubert et al. Pursuant To 35 U.S.C. § 103(a)</u>

Claims 2, 4, 5, 11, 13, 14, and 15 were rejected as being unpatentable over Assaderaghi in view of U.S. Patent No. 4,885,618 to Schubert et al. (hereinafter "Schubert"). Applicant respectfully disagrees with these rejections.

In order to reject a claim as obvious, the Examiner has the burden of establishing a *prima facie* case of obviousness. *In re Warner et al.*, 379 F.2d 1011, 154 USPQ 173, 177-178 (C.C.P.A. 1967). To establish a *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP § 2143.03.

For at least the reasons state above, Applicant submits that claim 1 is patentable over Assaderaghi.

Schubert does not appear to teach the combination of features of claim 1 including, but not limited to, the feature of: "wherein the thin silicon layer has a thickness between about 1 nm and about 50 nm". Schubert appears to teach a silicon oxide barrier. Schubert states, "formed oxide barrier 30 is placed under silicon substrate 42, as shown in Fig. 4B" (Column 5, lines 17 and 18).

Although, Assaderaghi and Schubert describe silicon layers, Applicant submits that Assaderaghi alone or in combination with Schubert do not appear to provide guidance in regards to a thickness of the silicon layer. Applicant submits that it is not obvious to one of ordinary skill in the art that a silicon layer having a thickness between about 1 nm and 50 nm will ensure a reliable and sufficient contact between the source and drain regions.

Portions of the aforementioned rejection appear to be set forth in facts within the personal knowledge of the Examiner and therefore Applicant believes MPEP 2144.03 will apply. Pursuant to MPEP 2144.03, Applicant respectfully requests the Examiner to provide support for his assertion either by an affidavit or by references brought to the Applicant's attention. Otherwise, Applicants request this rejection be removed. *See, e.g.*, MPEP 2143.01.

Applicant submits that the features of claim 1 including, but not limited to, the feature of: "wherein the thin silicon layer has a thickness between about 1 nm and about 50 nm" does not appear to be taught or suggested by Assaderaghi alone or in combination with Schubert. As such, Applicant submits that claim 1 is patentable over Assaderaghi in view of Schubert.

Claim 2 states in part, "wherein the buried dielectric layer extends between the source and drain regions." Applicant submits that the features of claim 2 in combination with the features of independent claim 1 do not appear to be taught or suggested by the cited art.

Claim 4 states in part, "wherein the device has a planar structure." Applicant submits that the features of claim 4 in combination with the features of independent claim 1 do not appear to be taught or suggested by the cited art.

Claim 5 states in part, "wherein the buried dielectric layer is an air-filled cavity." Applicant submits that the features of claim 5 in combination with the features of independent claim 1 do not appear to be taught or suggested by the cited art.

Claim 11 states in part, "wherein the buried dielectric layer has a thickness between about 1 nm and about 50 nm." Applicant submits that the features of claim 11 in combination with the features of independent claim 1 do not appear to be taught or suggested by the cited art.

Claim 13 states in part, "wherein a length of the two opposed zones is less than about 100 nm." Applicant submits that the features of claim 13 in combination with the features of independent claim 1 do not appear to be taught or suggested by the cited art.

Claim 14 states in part, "wherein the thin gate dielectric layer comprises SiO_2." Applicant submits that the features of claim 14 in combination with the features of independent claim 1 do not appear to be taught or suggested by the cited art.

Claim 15 states in part, "wherein the source and drain regions lie in the same plane as the gate." Applicant submits that the features of claim 15 in combination with the features of independent claim 1 do not appear to be taught or suggested by the cited art.

E. The Claims Are Not Obvious Over Assaderaghi In View of Schubert et al. Pursuant To 35 U.S.C. § 103(a)

Claim 20 was rejected as being unpatentable over Assaderaghi in view to Schubert. Applicant respectfully disagrees with this rejection.

Claim 20 describes a semiconductor device having a combination of features including, but not limited to, the features of: "wherein the thin silicon layer has a thickness between about 1 nm and about 50 nm."

For at least the reasons stated above, Applicant submits that the combination of features of the claim 20 are not taught or suggested by Assaderaghi alone or in combination with Schubert. As such, Applicant submits that claim 20 is patentable over Assaderaghi in view of Schubert.

F. Additional Comments

Favorable reconsideration is respectfully requested.

Applicant respectfully requests a two-month extension of time. A fee authorization is enclosed to cover the fee for the extension of time. If any additional extension of time is required, Applicant hereby requests the appropriate extension of time. If any additional fees are required or fees have been overpaid, please appropriately charge or credit those fees to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account Number 50-1505/5972-00300/EBM.

Respectfully submitted,

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